from the second region, the first and second interconnection structures have top surfaces in the upper portion of the semiconductor substrate, each of the top surfaces of the first and second interconnection structures is at the same level as or a different level from a top surface of the insulating layer.

According to another aspect, the inventive concept is directed to a semiconductor device including first and second interconnection structures. The first interconnection structure includes first and second buried patterns sequentially stacked in a first region of a semiconductor substrate to be parallel to a top surface of the semiconductor substrate, third and fourth buried patterns sequentially stacked on the second buried pattern to form a concave shape on the second buried pattern, and a fifth buried pattern disposed on the fourth buried pattern and surrounded by the third and fourth buried patterns. The second interconnection structure includes first and second stack patterns sequentially stacked in a second region of the semiconductor substrate to be parallel to the top surface of the semiconductor substrate, a third stack pattern having the concave shape on the second stack pattern and configured to extend from a top surface of the second stack pattern toward an upper portion of the semiconductor substrate, and a fourth stack pattern disposed on the third stack pattern and surrounded by the third stack pattern. The first buried pattern and the first stack pattern include insulating material, the second and third buried patterns and the second stack pattern include diffusion stopping material, the fourth buried pattern and the third stack pattern include work-function adjusting material, and the fifth buried pattern and the fourth stack pattern include power applying material.

In one embodiment, the semiconductor device further includes an insulating layer disposed on the semiconductor substrate. The insulating layer surrounds the first and second interconnection structures, the third through fifth buried patterns and the third and fourth stack patterns have substantially the same top surface in the upper portion of the semiconductor substrate, and the top surfaces of the third through fifth buried patterns and the third and fourth stack patterns are at substantially the same level as a top surface of the insulating layer.

In one embodiment, the semiconductor device further includes buried and stack capping patterns disposed in the first and second interconnection structures, respectively, and an insulating layer disposed on the semiconductor substrate and configured to surround the first and second interconnection structures. The third through fifth buried patterns and the third and fourth stack patterns have substantially the same top surface in the upper portion of the semiconductor substrate, the buried capping pattern is disposed on the third through fifth buried patterns, the stack capping pattern is disposed on the third and fourth stack patterns, and top surfaces of the buried and stack capping patterns are at substantially the same level as a top surface of the insulating layer.

In one embodiment, the semiconductor device further includes buried and stack capping patterns disposed in the first and second interconnection structures, respectively, and an insulating layer disposed on the semiconductor substrate and configured to surround the first and second interconnection structures. Upper portions of the third through fifth buried patterns protrude from a top surface of the insulating layer, extend to the top surface of the insulating layer, and are sequentially stacked to be parallel to the top surface of the semiconductor substrate, upper portions of the third and fourth stack patterns protrude from the top surface of the insulating layer, extend to the top surface of the insulating layer, and are sequentially stacked to be parallel to the top surface of the semiconductor substrate, the buried capping pattern is disposed on the fifth buried pattern, and the stack capping pattern is disposed on the fourth stack pattern.

In one embodiment, the semiconductor device further includes an insulating layer disposed on the semiconductor substrate and configured to surround the first and second interconnection structures. The third through fifth buried patterns have top surfaces disposed at the same level as or a different level from a top surface of the insulating layer in the upper portions of the semiconductor substrate, and the third and fourth stack patterns have top surfaces disposed at the same level as or a different level from the top surface of the insulating layer in the upper portions of the semiconductor substrate.

In one embodiment, the first region of the semiconductor substrate has a different conductivity type from the second region, and the insulating material includes one selected from the group consisting of hafnium-based material, lanthanide-based material, zirconium-based material, Pr_2O_3, Dy_2O_3, $Ba_XSr_YTiO_Z$ (BST) material and Pb(Zr, Ti)O_3 (PZT) material.

In one embodiment, a lower portion of the diffusion stopping material of the first interconnection structure includes one of binary-based metal nitride and ternary-based metal nitride, and an upper portion of the diffusion stopping material of the first interconnection structure includes one selected from the group consisting of HfAlN, HfSiN, TaAlN, TaSiN, TiAlN and TiSiN.

In one embodiment, a lower portion of the diffusion stopping material of the first interconnection structure includes one of binary-based metal nitride and ternary-based metal nitride, and an upper portion of the diffusion stopping material of the first interconnection structure includes silicon nitride, silicon carbide or silicide of one selected from the group consisting of hafnium (Hf), molybdenum (Mo), tantalum (Ta), titanium (Ti) and tungsten (W).

In one embodiment, the diffusion stopping material of the second interconnection structure includes one of binary-based metal nitride and ternary-based metal nitride, or silicide nitride, silicon carbide or silicide of one selected from the group consisting of Hf, Mo, Ta, Ti and W.

In one embodiment, the work-function adjusting material is carbide, nitride, silicon nitride or silicide of one selected from the group consisting of Hf, Mo, Ta, Ti and W, or is one selected from the group consisting of platinum (Pt), ruthenium (Ru), iridium oxide (IrO) and ruthenium oxide (RuO), and the power applying material includes aluminum (Al) or a combination of Al and Si.

According to another aspect, the inventive concept is directed to a semiconductor module comprising a module substrate and at least one semiconductor package structure electrically connected to the module substrate and including at least one semiconductor device. The at least one semiconductor device comprises at least one complementary metal-oxide-semiconductor (CMOS) transistor disposed in a semiconductor substrate, and the at least one CMOS transistor comprises: a first interconnection structure disposed in a first region of the semiconductor substrate and configured to extend from a top surface of the semiconductor substrate toward an upper portion thereof; and a second interconnection structure disposed in a second region of the semiconductor substrate and configured to extend from the top surface of the semiconductor substrate toward the upper portion thereof. Each of the first and second interconnection structures includes insulating material, diffusion stopping material, work-function adjusting material, and power